

A 90 GHz Amplifier Assembled Using Flip-Chip Technology

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Abstract:

This letter reports the performance of a novel single-stage W-band amplifier fabricated utilizing flip-chip bump-bonding. We have bump-bonded a high-speed, low-noise InP high electron mobility transistor (HEMT) device onto a separately fabricated passive circuit having a GaAs substrate. This new *quasi*-monolithic millimeter-wave integrated circuit (Q-MMIC) amplifier exhibits a peak gain of 5.8 dB at ~90 GHz and a 3 dB bandwidth of greater than 25%. Our bump-bonding technique is a useful alternative to the high cost of monolithic millimeter-wave integrated circuits (MMIC's), and does not compromise frequency performance, at least up to 100 GHz.

Key words:

Gallium compounds, Indium compounds, Coplanar waveguides, Flip-chip devices, Millimeter wave amplifiers, Millimeter wave circuits, Millimeter wave FET amplifiers, Millimeter wave FETs, Millimeter wave integrated circuits, Millimeter wave measurements, Millimeter wave technology, Millimeter wave transistors, Bump-bonding

1) **Introduction:**

Two main approaches to millimeter-wave flip-chip circuits have been attempted in the literature. In one case, complete monolithic microwave integrated circuit (MMIC) chips are bonded to dielectric substrates, in order to realize complex millimeter-wave systems [1, 2]. In the second case, discrete components only (diode mixers, capacitors, FETs, etc.) are bonded onto a substrate with passive circuitry[3,4]. Both methods have demonstrated their potential as alternatives to pure MMIC's. Our work follows the second approach, as in [3], where *only* the active device is bump-bonded to a passive MMIC. We will refer to this type of circuit as a bump-bonded *quasi*-monolithic millimeter-wave circuit (Q-MMIC).

For many millimeter-wave applications, the use of bump-bonding technology to assemble discrete components into Q-MMICs offers several advantages such as:

- a) Lower cost associated with conserving the expensive semiconductor area for the active device fabrication, while using cheaper substrates for the more expansive passive circuitry.
- b) Higher overall performance and yield of the final circuits by pre-screening components prior to assembly. Device variations associated with wafer-to-wafer and lot-to-lot process control are eliminated, as the passive circuitry can be tuned for already-existing transistors.
- c) The flexibility to mix and match components for circuit fabrication.
- d) Additionally, because the discrete devices and the circuits are fabricated separately, the processes for each component can be less complex, thus simplifying the fabrication process. By hybridizing the best-available active devices on passive circuits with a bump-bonding technique, Q-MMICs can provide some of the flexibility of discrete microwave integrated circuits (MIC's) with the performance advantage of MMIC's, for very short turnaround times, low cost of fabrication, and uncompromised frequency performance.

In this paper, we present the results of bump-bonding InP HEMT's onto a coplanar waveguide (CPW) passive circuit. Our objective is to fabricate 100 GHz and higher low-noise amplifiers (LNA's) using an already existing InP HEMT inventory. Our first LNA circuit with a single InP HEMT has

shown a peak gain of 5.8 dB at approx. 90 GHz, and gain up to 117 GHz. To our knowledge, this is the highest frequency amplifier assembled with a bump-bonding technique.

2) **Experimental Procedure:**

The discrete transistors used in the work are InP HEMTs employing a pseudomorphic InGaAs channel with 80% indium composition and gate lengths of 0.1 μm [5,6]. A photograph is shown in Figure 1. The device area and pad size are intentionally small to reduce parasitics. Different device topologies of two and four fingers, and varying unit gate width of 10 and 20 μm were examined. The current-voltage (I - V) characteristics for a typical InP HEMT bonded to a 50 Ω CPW line are shown in Figure 2. The I - V curves did not change significantly through the bump-bonding process. The devices exhibited good pinchoff characteristics with typical transconductances of 1000 mS/mm and threshold voltages between -250 and -300 mV.

The passive circuits have been fabricated on a 635 μm thick semi-insulating GaAs substrate. While we expect this bump-bonding technique to work on other commonly used passive low loss substrates, GaAs was chosen for ease of fabrication in our laboratory. A cluster of six electroplated bumps is incorporated onto the amplifier's passive circuit for the purpose of attaching the HEMT onto the bumps. The bump process has 1-2 μm of alignment accuracy. The bumps are fabricated by electroplating layers of Au and Sn with thicknesses of 7 μm and 3 μm , respectively. After heating to 400° C in a rapid thermal annealer, the Sn layer partially consumes part of the Au to form a Au/Sn eutectic on top of each bump[7]. The bumps are approximately 16 μm wide, 40 μm long and 8 μm high, with the size based on the bond pads on the existing devices. The discrete device and the passive circuit were bonded at a 370 °C heater temperature with a force of 0.03 N/bump using a bonding system from Research Devices [7]. The device temperature through the bonding process was not measured.

Shear tests were performed on the bump-bonded Q-MMIC, using a die shear military standard with a minimum force requirement of 0.04 kg/10⁻⁴ in² (for a die area smaller than 5⁻⁴ in²). For our bump bond configuration, the total bond area for all six bumps is 6 x 16 x 40 μm^2 = 3840 μm^2 = 5.95 x 10⁻⁶

in², yielding a minimum shear force requirement of 2.38 grams. The Q-MMIC failed at 6.9 grams, exceeding the military specification by almost a factor of three.

Figure 3a shows a close-up picture of the passive circuit of the W-band amplifier, before bump-bonding the InP HEMT. Figure 3b shows an equivalent circuit of the amplifier, which incorporates a pair of matching stubs terminated by capacitors. In the design of the amplifier, we used the model for a device with four 10 μm -wide gate fingers, even though our best device had only two 20 μm -wide gate fingers, as we did not have an available model for the two-finger device. This amplifier design did not include any corrections for the extra inductance and capacitance that are inherently associated with bump-bonding the devices. Our objective was to create the simplest amplifier possible to demonstrate the bump-bonding technique at millimeter-wave frequencies. Bias circuitry was not included in the design; instead, bias was applied through the input and output probes used in the measurement. We used MMICAD to simulate the amplifier performance.

3) Results

Frequency response measurements were performed on these circuits between 85-120 GHz. This frequency band was measured using frequency extension modules manufactured by Oleson Microwave Labs. Figure 4 shows the measured and simulated magnitude of S-parameters from 85-120 GHz, of the two-finger InP HEMT bump-bonded to the LNA passive circuit of Figure 3a. The maximum gain is 5.8 dB at ~ 90 GHz, and gain extends to 117 GHz. The measured gain agrees well with the design in the center of the band, and the agreement falls off at the band edges. We expect that at least some of the discrepancy between the measured and modeled data is a result of using a model for a similar (same periphery) but nonetheless *different* device. However, the good agreement in band suggests that the device model inaccuracies are small. In addition, since no accommodation for the bump-bonding parasitics was made in the design, the result implies that the parasitic elements associated with the bonding itself do not dominate the performance of the LNA circuit. The reason for this may be the small ~ 8 μm bump height. Note also that the small physical size of the transistor chip minimizes the capacitive parasitics and resonant modes in the InP substrate. We expect that the significance of the

bump parasitics will become more important as we design higher frequency amplifiers, however, at this time we have *not* exhausted the limits of our bump technology.

4) **Conclusion**

In this work, we demonstrated a single-stage W-band amplifier fabricated by bump bonding a discrete InP HEMT to a passive matching circuit. The 85 to 120 GHz frequency measurement of an amplifier designed with a two 20 μm gate finger HEMT shows nearly 6 dB of gain and a wide bandwidth at 90 GHz. Measured and modeled performances are very similar. With further investigation and more accurate device models, it should be possible to assemble higher frequency, more complex, multi-stage amplifiers with Q-MMIC technology.

5) **Acknowledgments**

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References:

- [1] M. Ito, K. Maruhashi, H. Kusamitsu, Y. Morishita, and K. Ohata, "Analysis of Flip-chip MMIC Structure for 60-and 76-GHz Low Noise Amplifiers," in *Proc. Asia-Pacific Microwave Conf.*, 1998, p. 299.
- [2] Wolfgang Menzel, "Interconnect and Packaging Techniques for Complex Millimeter Wave Front-Ends," in *Proc. Asia-Pacific Microwave Conf.*, 1998, p. 283.
- [3] R. S. Virk, S. A. Maas, M. G. Case, M. Matloubian, P. Lawyer, H. C. Sun, C. Ngo, and D. B. Rensch, "A Low-Cost W-Band MIC Mixer Using Flip-Chip Technology," *IEEE Microwave and Guided Wave Lett.*, vol. 7, no. 9, pg. 294, 1997.
- [4] Y. Arai, M. Sato, H. T. Yamada, T. Hamada, K. Nagai, and H. I. Fujishiro, "60-GHz Flip-Chip Assembled MIC Design Considering Chip-Substrate Effect," *IEEE Trans. on Microwave Theory Tech.*, vol. 45, pg. 2261, 1997.
- [5] M. Wojtowicz, R. Lai, D. C. Streit, G. I. Ng, T. R. Block, K. L. Tan, P. H. Liu, A. K. Freudenthal, and R. M. Dia, "0.10 μm graded InGaAs channel InP HEMT with 305 GHz f_T and 340 GHz f_{max} ," *IEEE Electron Device Lett.*, vol. 15, no. 11, pg. 477, 1994.
- [6] Similar devices with four 20 μm wide gate fingers were used to build state-of-art cryogenically cooled MIC amplifiers at 30 GHz with 9-10 K noise temperature (private communication with Todd Gaier).
- [7] J. H. Lau, "Flip Chip Technologies," McGraw-Hill, New York, 1995.

Figure Captions:

- 1) An InP HEMT with two 20 μm gate fingers with gate lengths of 0.1 μm . Source pads are on the top and bottom, the gate pad is on the left, and the drain is on the right. The marks on the pads are from routine screening with wafer probes. The chip dimensions are approximately 175 μm x 200 μm x 75 μm thick.
- 2) Current-voltage characteristics of a device similar to Figure 1, bump bonded onto a CPW 50 Ohm line. The gate voltage (V_{gs}) steps are from -300 to 300 mV in increments of 50 mV/step. This device has a peak g_m of approximately 1000 mS/mm and a V_t of -300 mV. The other devices from this same wafer exhibit similar current-voltage characteristics.
- 3) a) The passive W-band LNA circuit. The electroplated Au/Sn bumps in the center are used for fluxless bump bonding. The gate and drain matching capacitors are connected to the CPW transmission lines through series air bridges. b) Equivalent circuit. The ends of the input and the output CPW transmission line are matched to 50 Ω impedances.
- 4) Magnitude of the measured and modeled S-parameters for the W-band LNA. The bias conditions were $V_{gs} = 0.1$ V, $V_{ds} = 1$ V, and $I_{ds} = 11$ mA.

Figure 1

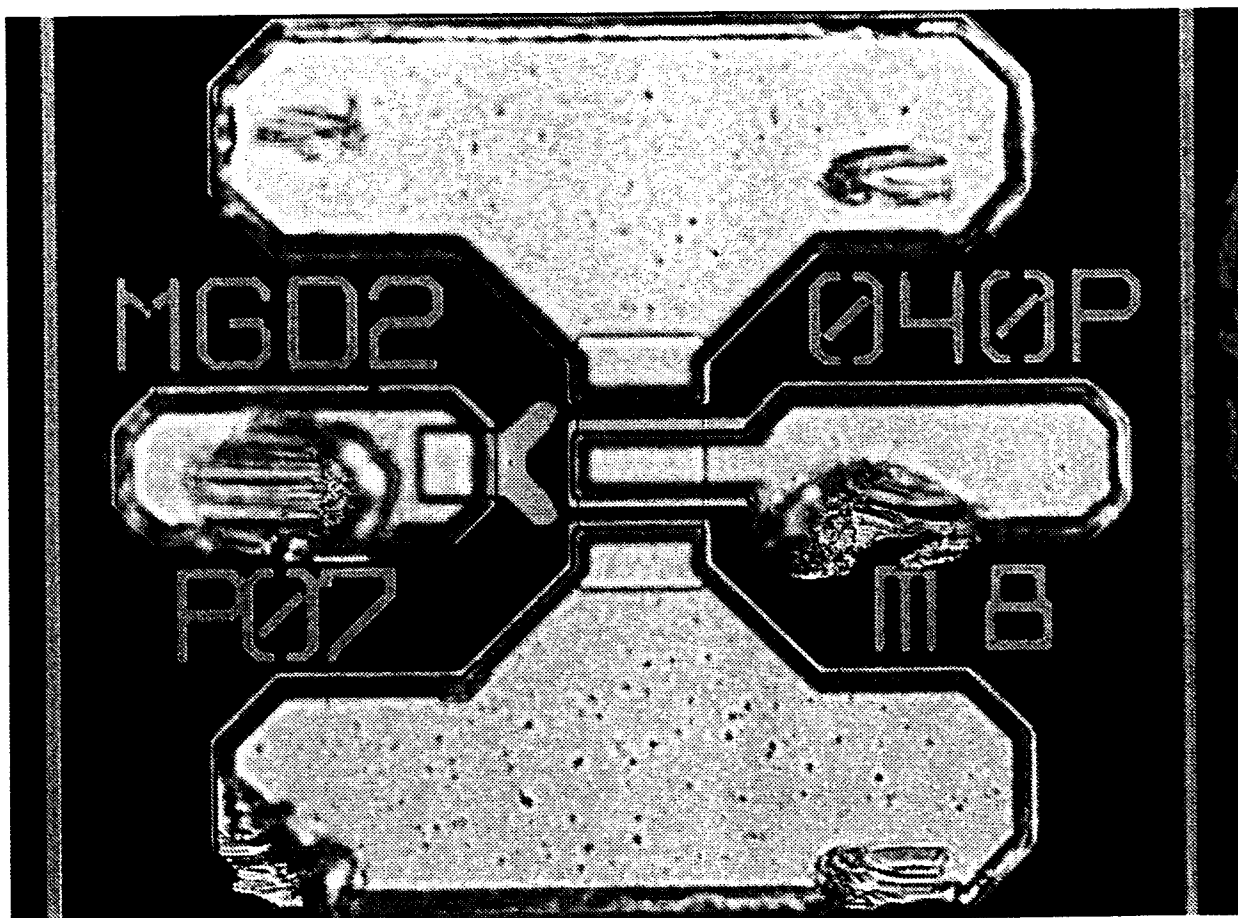


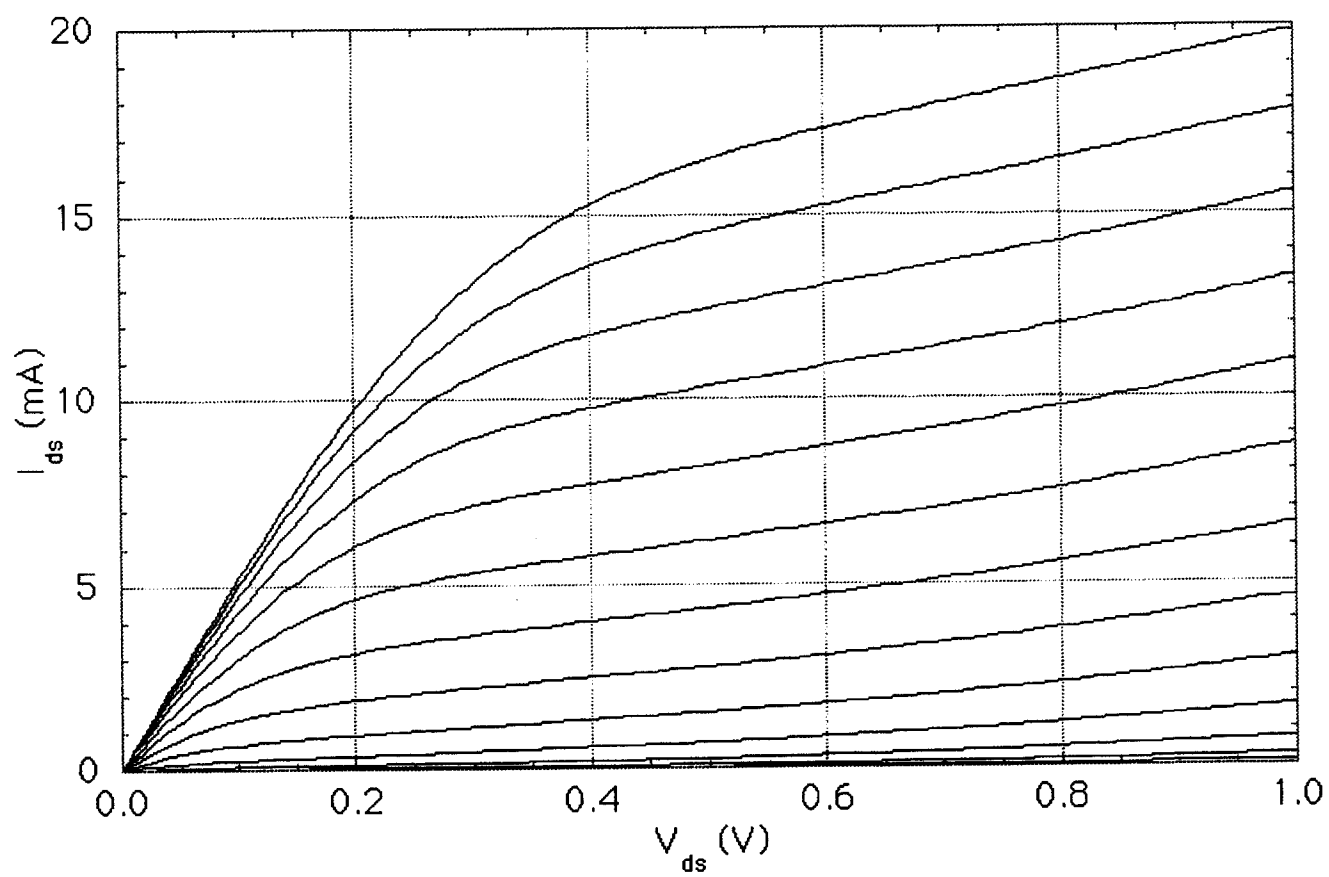
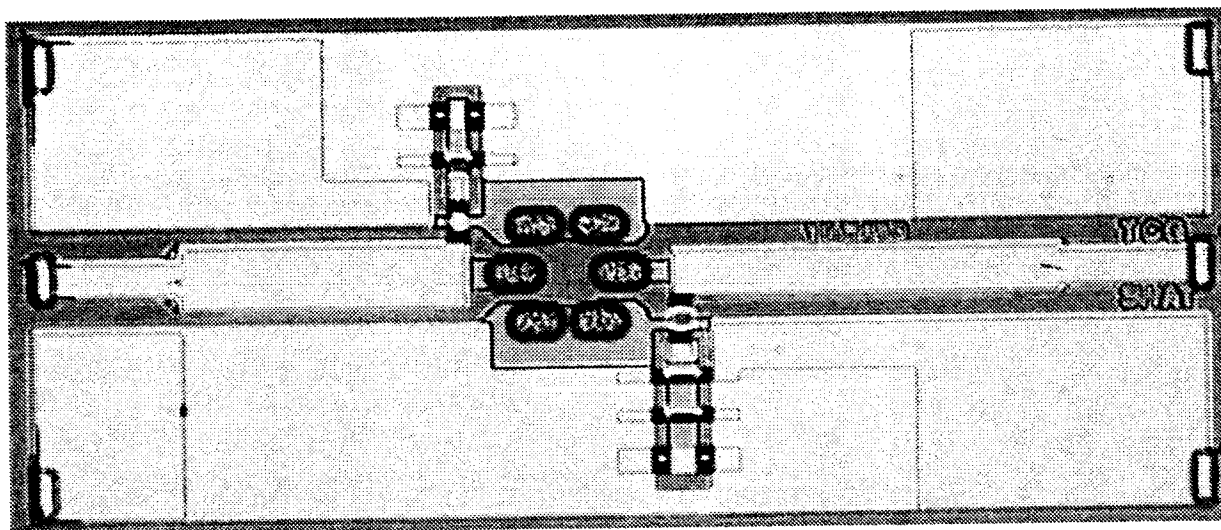
Figure 2

Figure 3

a)



b)

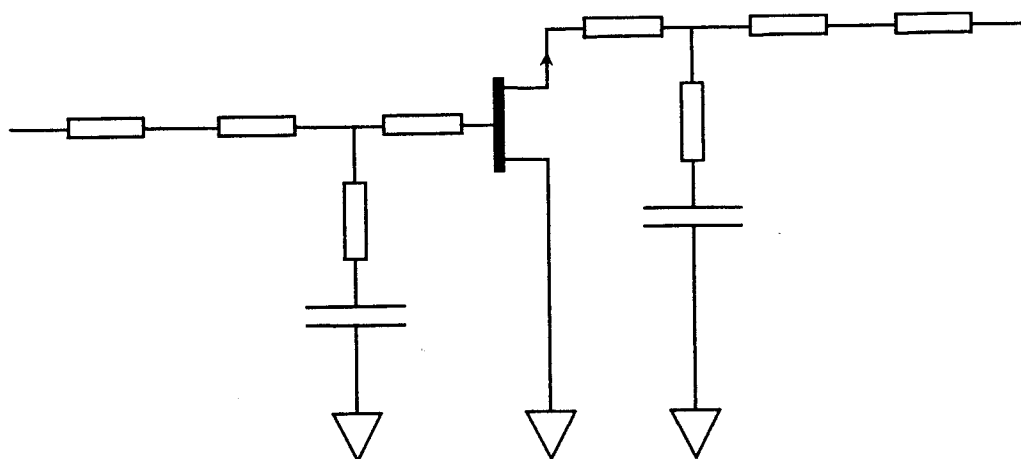


Figure 4